REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-6 are in this case. Claims 1, 2, 4 and 5 have been rejected under § 102(e). Claims 3 and 6 have been rejected under § 103(a). Claims 3 and 6 have been canceled. Independent claims 1 and 4 have been amended. New claims 7-11 have been added.

The claims before the Examiner are directed toward a system and method for recording data in a multi-board solid-state storage system. The system includes a main board and at least one memory board, each of which has primary and secondary non-volatile memory. The secondary memory of each board is used to store records of faulty locations of the board's primary memory.

§ 102(e) Rejections – Ajanovic '426

The Examiner has rejected claims 1, 2, 4 and 5 under § 102(e) as being anticipated by Ajanovic, US Patent No. 6,298,426 (henceforth, "Ajanovic '426"). The Examiner's rejection is respectfully traversed.

As discussed below in the context of the § 103(a) rejections, claim 1 now has been amended to include some of the limitations of claim 3 and claim 4 now has been amended to include some of the limitations of claim 6. These amendments render moot the § 102(e) rejections.

§ 103(a) Rejections – Ajanovic '426 in view of Jeddeloh '798 and Okaue et al. '140

The Examiner has rejected claims 3 and 6 under § 103(a) as being unpatentable over Ajanovic '426 in view of Jeddeloh, US Patent No. 6,052,798

(henceforth, "Jeddeloh '798") and in further view of Okaue et al., US Patent No. 6,601,140 (henceforth, "Okaue et al. '140"). The Examiner's rejection is respectfully traversed.

Strictly speaking, claims 3 and 6 now have been canceled, thereby rendering moot the Examiner's rejection of these claims. However, as discussed below, claims 1 and 4 have been amended to include some of the limitations of claims 3 and 6. Therefore, the following discussion is directed towards the patentability of claims 1 and 4, as now amended, over the combination of Ajanovic '426 with Jeddeloh '798 or Okaue et al. '140.

Ajanovic '426 teaches a computer system whose main memory **106** includes four (Figure 2) or three (Figure 3) volatile memory modules (DIMMs) **200** or **300** that plug into the motherboard. Each memory module includes a nonvolatile NVRAM **201** or **301** for storing information about the memory module such as (column 3 lines 65-66):

...memory data width, ECC, memory size, DRAM or SDRAM.

Claims 1 and 4 could be construed as reading on the teachings of Ajanovic '426.

The Examiner has cited Okaue et al. '140 as rendering obvious one of the limitations (including security information in the system information) recited in dependent claims 3 and 6 as filed, and Jeddeloh '798 as rendering obvious another of the limitations (including faulty location records in the system information) recited in dependent claims 3 and 6 as filed.

Applicant has rendered moot the rejection of claims 3 and 6 as unpatentable over the combination of Ajanovic '426 and Okaue et al. '140 by amending claims 1 and 4 to recite the recording of "faulty location records" in the secondary nonvolatile memory devices, thereby requiring the inclusion of faulty location records in the

system information stored in the secondary nonvolatile memory devices. Support for this amendment is found in claims 3 and 6 as filed. Correspondingly, claims 3 and 6 have been canceled. In addition, the "storing" step of claim 4 has been deleted as redundant. It remains to be shown that claims 1 and 4 are patentable over the combination of Ajanovic '426 and Jeddeloh '798.

Jeddeloh '798 teaches a computer system 10 that includes a memory module **12**. Memory module **12** has a volatile memory block **14** and a nonvolatile memory block **16** that stores a map **18** of defective portions of volatile memory block **14**. One ordinarily skilled in the art, upon reading column 2 lines 61-65 of Jeddeloh '798:

> The volatile memory block **14** preferably includes one or more dynamic random access memory (DRAM) chips, but the invention is equally applicable for other types of volatile memory, such as static random access memory (SRAM). (emphasis added)

would be led to not apply the teachings of Jeddeloh '798 to the storage of faulty location records of nonvolatile primary memory in an associated secondary memory. Therefore, claims 1 and 4 have been amended to limit the primary solid-state components to non-volatile memory devices. Support for this amendment is found in the specification on page 5 line 21 through page 6 line 2:

> The components of the present invention are:
> ...ii) Multiple boards carrying primary solid-state components (such as Flash, RAM, EEPROM); (emphasis added)

As is well known in the art, Flash memory and EEPROM are non-volatile.

In addition, new claims 7 and 8 have been added to limit the primary solid-state components to Flash memory devices. Support for new claims 7 and 8 is found in the above citation from page 5 line 21 through page 6 line 2.

With independent claims 1 and 4 allowable in their present form, it follows that claims 2, 5, 7 and 8, that depend therefrom, also are allowable.

Other New Claims

New claims 9-11 have been added. These claims recite an aspect of the present invention that is described in the specification on page 11 lines 8-15: recording faulty location records in each of two areas of the secondary non-volatile memory device of each memory board, and subsequently updating the faulty location records of one of the areas with records of failures during system operation.

New independent claim 9 lacks the limitation, now present in claims 1 and 4 as amended, that the faulty location records are of non-volatile memory devices. Nevertheless, new claim 9 is patentable over the prior art cited by the Examiner. There is neither a hint nor a suggestion in the prior art cited by the Examiner of any utility to storing a faulty location record twice in two different locations of a secondary non-volatile memory. New claims 10 and 11 are patentable over the prior art cited by the Examiner by virtue of depending from new claim 9.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 4 and 9, and hence dependent claims 2, 5, 7, 8, 10 and 11 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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